Amendments to the Claims

Please amend the claims as follows:

1. (currently amended) A pipeline accelerator, comprising:

a memory; and

a hardwired-pipeline circuit coupled to the memory, including at least one processing pipeline, and operable to,

receive a message that includes data and that includes a header having information indicating a destination of the data,

extract the data from the message,

load the extracted data into the memory,

retrieve the extracted data from the memory,

process the retrieved data with a pipeline corresponding to the destination, and

provide the processed data to an external source.

2. (original) The pipeline accelerator of claim 1 wherein:

the memory is disposed on a first integrated circuit; and

the pipeline circuit is disposed on a second integrated circuit.

3. (original) The pipeline accelerator of claim 1 wherein the pipeline circuit is disposed on a field-programmable gate array.

4. (original) The pipeline accelerator of claim 1 wherein the pipeline circuit is operable to provide the processed data to the external source by:

loading the processed data into the memory;

retrieving the processed data from the memory; and

providing the retrieved processed data to the external source.

5. (original) The pipeline accelerator of claim 1 wherein:

the external source comprises a processor; and

the pipeline circuit is operable to receive the data from the processor.

6. (Currently amended) A computing machine, comprising:

a processor operable to broadcast a message that includes data and that includes a header having a information indicating a destination of the data; and

a pipeline accelerator coupled to the processor and comprising,

a memory, and

a hardwired-pipeline circuit coupled to the memory, including at least one processing pipeline, and operable to,

receive the message~~data~~ from the processor,

extract the data from the message,

load the extracted data into the memory,

retrieve the extracted data from the memory,

process the retrieved data with a pipeline corresponding to the destination, and

provide the processed data to the processor.

7. (Currently amended) A pipeline accelerator, comprising:

a memory; and

a hardwired-pipeline circuit coupled to the memory and operable to,

receive data,

process the received data,

load the processed data into the memory,

retrieve the processed data from the memory,

generate a message header that includes first information indicating a destination of the processed data;

generate a message that includes the processed data and the header; and

provide the message~~retrieved processed data~~ to an external source.

8. (Currently amended) A computing machine, comprising:

a processor operable to run at least one software application; and

a pipeline accelerator coupled to the processor and comprising,

a memory, and

a hardwired-pipeline circuit coupled to the memory and operable to,

receive data from the processor,

process the received data,

load the processed data into the memory,

generate a message header that includes for the processed data information that indicates a destination software application running on the processor,

retrieve the processed data from the memory,

generate a message that includes the retrieved processed data and the message header, and

provide the message ~~retrieved processed data~~ to the processor.

9. (Currently amended) A pipeline accelerator, comprising:

first and second memories; and

a hardwired-pipeline circuit coupled to the first and second memories and comprising,

an input-data handler operable to receive ~~raw data~~ from an external source a first message that includes raw data and that includes a first header having information indicating a destination of the raw data, to extract the raw data from the message, and to load the raw data into the first memory,

at least one hardwired pipeline operable to process ~~the raw~~ data,

a pipeline interface operable to retrieve the raw data from the first memory, provide the retrieved raw data to ~~the~~ a hardwired pipeline corresponding to the destination, and load processed data from the hardwired pipeline into the second memory, and an output-data handler operable to retrieve the processed data from the second memory, to generate a second header having first information indicating a destination of the processed data, to generate a second message that includes the processed data and the second header, and to provide the second message~~processed data~~ to the external source.

10. (original) The pipeline accelerator of claim 9 wherein:

the first and second memories each include respective first and second ports;

the input-data handler is operable to load the raw data via the first port of the first memory,

the pipeline interface is operable to retrieve the raw data via the second port of the first memory and to load the processed data via the first port of the second memory, and

the output-data handler is operable to retrieve the processed data via the second port of the second memory.

11. (original) The pipeline accelerator of claim 9, further comprising:

a third memory coupled to the hardwired-pipeline circuit;

wherein the hardwired pipeline is operable to generate intermediate data while processing the raw data; and

wherein the pipeline interface is operable to load the intermediate data into the third memory and to retrieve the intermediate data from the third memory.

12. (original) The pipeline accelerator of claim 9 wherein:

the first and second memories are respectively disposed on first and second integrated circuits; and

the pipeline circuit is disposed on a field-programmable gate array.

13. (original) The pipeline accelerator of claim 9, further comprising:

an input-data queue coupled to the input-data handler and the pipeline interface;

wherein the input-data handler is operable to load into the input-data queue a pointer to a location of the raw data within the first memory; and

wherein the pipeline interface is operable to retrieve the raw data from the location using the pointer.

14. (original) The pipeline accelerator of claim 9, further comprising:

an output-data queue coupled to the output-data handler and the pipeline interface;

wherein the pipeline interface is operable to load into the output-data queue a pointer to a location of the processed data within the second memory; and

wherein the output-data handler is operable to retrieve the processed data from the location using the pointer.

15. (original) The pipeline accelerator of claim 9, further comprising:

wherein each of the input-data handler, hardwired pipeline, pipeline interface, and output-data handler has a respective operating configuration; and

a configuration manager coupled to and operable to set the operating configurations of the input-data handler, hardwired pipeline, pipeline interface, and output-data handler.

16. (original) The pipeline accelerator of claim 9, further comprising:

wherein each of the input-data handler, hardwired pipeline, pipeline interface, and output-data handler has a respective operating status; and

an exception manager coupled to and operable to identify an exception in the input-data handler, hardwired pipeline, pipeline interface, or output-data handler in response to the operating statuses.

17. – 40. Cancelled.

41. (Currently amended) A method, comprising:

receiving a message that includes data and that includes a header having information indicating a destination of the data;

extracting the data from the message;

loading the extracted data into a memory;

retrieving the extracted data from the memory;

processing the retrieved data with a hardwired-pipeline circuit that corresponds to the destination of the data; and

providing the processed data to an external source.

42. (original) The method of claim 41 wherein providing the processed data comprises:

loading the processed data into the memory;

retrieving the processed data from the memory; and

providing the retrieved processed data to the external source.

43. (Currently amended) A method, comprising:

processing data with a hardwired-pipeline circuit;

loading the processed data into a memory;

retrieving the processed data from the memory;

generating a header having first information indicating a destination of the processed data;

forming a message from the header and the processed data; and

providing the message~~retrieved processed data~~ to an external source.

44. (Currently amended) A method, comprising:

receiving from an external source a first message that includes raw data and that includes a first header having information indicating a destination of the raw data;

extracting the raw data from the message;

loading the extracted raw data ~~from an external source~~ into a first memory;

retrieving the extracted raw data from the first memory;

processing the retrieved data with a hardwired pipeline;

loading the processed data from the hardwired pipeline into a second memory;

generating a second header having information indicating a destination of the processed data;

retrieving the processed data from the second memory;

generating a second message that includes the processed data and the second header; and

providing the second message~~processed data from the second memory~~ to the external source.

45. (original) The method of claim 44 wherein:

loading the raw data comprises loading the raw data via a first port of the first memory;

retrieving the raw data comprises retrieving the raw data via a second port of the first memory;

loading the processed data comprises loading the processed data via a first port of the second memory; and

providing the processed data comprises retrieving the processed data via a second port of the second memory.

46. (original) The method of claim 44, further comprising:

generating intermediate data with the hardwired pipeline in response to processing the raw data;

loading the intermediate data into a third memory; and

providing the intermediate data from the third memory back to the hardwired pipeline.

47. (original) The method of claim 44, further comprising:

loading into an input-message queue a pointer to a location of the raw data within the first memory; and wherein retrieving the raw data comprises retrieving the raw data from the location using the pointer.

48. (original) The method of claim 44, further comprising:

loading into an output-message queue a pointer to a location of the processed data within the second memory; and

wherein retrieving the processed data comprises retrieving the processed data from the location using the pointer.

49. (original) The method of claim 44, further comprising setting parameters for loading and retrieving the raw data, processing the retrieved data, and loading and providing the processed data.

50. (original) The method of claim 44, further comprising determining whether an error occurs during the loading and retrieving of the raw data, the processing of the retrieved data, and the loading and providing of the processed data.

51. – 65. Cancelled.

66. (new) The pipeline accelerator of claim 1 wherein the hardwired-pipeline circuit is further operable to:

extract from the header the information indicating the destination of the data;

generate from the extracted information an identifier that identifies the pipeline corresponding to the destination;

store the identifier in association with the data; and

provide the retrieved data to the pipeline in response to the stored identifier.

67. (new) The pipeline accelerator of claim 1 wherein the hardwired-pipeline circuit is further operable to:

extract from the header the information indicating the destination of the data;

generate from the extracted information an identifier that identifies the pipeline corresponding to the destination;

store a pointer to the extracted data;

store the identifier in association with the pointer; and

provide the retrieved data to the pipeline in response to the stored pointer and identifier.

68. (new) The pipeline accelerator of claim 1 wherein the hardwired-pipeline circuit is further operable to:

extract from the header the information indicating the destination of the data;

store a pointer to the extracted data in a location associated with the pipeline corresponding to the destination; and

provide the retrieved data to the pipeline in response to the stored pointer.

69. (new) The pipeline accelerator of claim 7 wherein the hardwired-pipeline circuit is further operable to:

store in association with the processed data second information indicating the destination of the processed data;

generate the message header in response to the second information.

70. (new) The pipeline accelerator of claim 69 wherein the second information equals the first information.

71. (new) The pipeline accelerator of claim 7 wherein the hardwired-pipeline circuit is further operable to:

store a pointer to the processed data;

store in association with the pointer second information indicating the destination of the processed data;

retrieve the processed data in response to the pointer; and

generate the message header in response to the second information.

72. (new) The pipeline accelerator of claim 7 wherein the hardwired-pipeline circuit is further operable to:

store a pointer to the processed data in a location associated with destination of the processed data;

retrieve the processed data in response to the pointer; and

generate the message header in response to the location.

73. (new) The pipeline accelerator of claim 9 wherein:

the input-data handler is further operable to,

extract from the header the information indicating the destination of the data,

generate from the extracted information an identifier that identifies the pipeline corresponding to the destination, and

store the identifier in association with the data; and

wherein the pipeline interface is further operable to provide the retrieved data to the pipeline in response to the stored identifier.

74. (new) The pipeline accelerator of claim 9 wherein:

the input-data handler is further operable to,

extract from the header the information indicating the destination of the data,

generate from the extracted information an identifier that identifies the pipeline corresponding to the destination,

store a pointer to the extracted data, and

store the identifier in association with the pointer; and

wherein the pipeline interface is further operable to provide the retrieved data to the pipeline in response to the stored pointer and identifier.

75. (new) The pipeline accelerator of claim 9 wherein:

the input-data handler is further operable to, extract from the header the information indicating the destination of the data,

store a pointer to the extracted data in a location associated with the pipeline corresponding to the destination; and

wherein the pipeline interface is further operable to provide the retrieved data to the pipeline in response to the stored pointer.

76. (new) The pipeline accelerator of claim 9 wherein:

the pipeline interface is further operable to store in association with the processed data second information indicating the destination of the processed data; and

the output-data handler is further operable to generate the first information from the second information.

77. (new) The pipeline accelerator of claim 76 wherein the second information equals the first information.

78. (new) The pipeline accelerator of claim 9 wherein:

the pipeline interface is further operable to

store a pointer to the processed data, and

store in association with the pointer second information indicating the destination of the processed data; and

the output-data handler is further operable to

retrieve the processed data in response to the pointer, and

generate the first information from the second information.

79. (new) The pipeline accelerator of claim 9 wherein:

the pipeline interface is operable to store a pointer to the processed data in a location associated with destination of the processed data; and

the output-data handler is further operable to

retrieve the processed data in response to the pointer, and

generate the first information in response to the location.

80. (new) The method of claim 41, further comprising:

extracting from the header the information indicating the destination of the data;

generating from the extracted information an identifier that identifies the hardwired-pipeline circuit corresponding to the destination;

storing the identifier in association with the data; and

provide the retrieved data to the hardwired-pipeline circuit in response to the stored identifier.

81. (new) The method of claim 41, further comprising:

extracting from the header the information indicating the destination of the data;

generating from the extracted information an identifier that identifies the hardwired-pipeline circuit corresponding to the destination;

storing a pointer to the extracted data;

storing the identifier in association with the pointer; and

providing the retrieved data to the hardwired-pipeline circuit in response to the stored pointer and identifier.

82. (new) The method of claim 41, further comprising:

extracting from the header the information indicating the destination of the data;

storing a pointer to the extracted data in a location associated with the hardwired-pipeline circuit corresponding to the destination; and

providing the retrieved data to the hardwired-pipeline circuit in response to the stored pointer.

83. (new) The method of claim 43, further comprising:

storing in association with the processed data second information indicating the destination of the processed data; and

wherein generating the header comprises generating the header in response to the second information.

84. (new) The method of claim 43, further comprising:

storing a pointer to the processed data;

storing in association with the pointer second information indicating the destination of the processed data;

retrieving the processed data in response to the pointer; and

wherein generating the header comprises generating the header in response to the second information.

85. (new) The method of claim 43, further comprising:

storing a pointer to the processed data in a location associated with the destination of the processed data;

retrieving the processed data in response to the pointer; and

wherein generating the header comprises generating the header in response to the location.